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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,292	01/29/2004	Hai Cong	CS2003/016	4993

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THE LAW OFFICES OF MIKIO ISHIMARU  
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SUITE 330  
SUNNYVALE, CA 94087

EXAMINER

GURLEY, LYNNE ANN

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/767,292

**Applicant(s)**

CONG ET AL.

**Examiner**

Lynne A. Gurley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-30 and 33-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 and 33-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
LYNNE A. GURLEY

**PRIMARY PATENT EXAMINER**  
**TC 2800, AU 2812**

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This Office Action is in response to the remarks filed 7/7/06.

Currently, claims 1-30 and 33-35 (new) are pending.

#### ***Response to Amendment***

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

#### ***Response to Arguments***

2. Applicant's arguments, see remarks, filed 7/7/06, with respect to the rejection(s) of claim(s) 1-30 and 33-35 under Weidman et al. (US 2003/0176058) in view of Wang et al. (US 2005/0110152) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Burke et al. (US 2005/0186782) in view of Weidman et al. (US 2003/0176058) and further in view of Wang et al. (US 2005/0110152).

#### ***Specification***

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-30 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burke et al. (US 2005/0186782, dated 825/05, filed 12/23/02) in view of Weidman et al. (US

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2003/0176058, dated 9/18/03, field 3/18/02) and further in view of Wang et al. (US

2005/0110152, dated 5/26/05, effectively filed 11/13/02).

6. Burke shows the method as claimed in figures 3A-3K and corresponding text, as providing a substrate with an insulating layer 304 over the substrate; providing a first level of conducting material 305 defined and embedded in the insulating layer over the substrate (fig. 3A); depositing an IMD layer 310/312/314/316 over the insulating layer; forming a bi-layered hard mask (318/320) over the IMD, the hard mask comprising a first layer (BARC 320) overlying a second hard mask layer HM2 (silicon oxide capping layer 318; [0038]), patterning the IMD layer and hard mask layers, and etching to form via openings extending through the IMD and the hard mask layers (Fig. 3E); forming a layer of via-fill material of BARC coating 326, the via-fill material filling the via openings (fig. 3G); patterning the via-fill material, IMD and hard mask layers, and etching to form trench openings (fig. 3I); and stripping-off the via-fill material after forming the trench openings (figs. 3I,3J), thus forming open trench and open via regions for subsequent conducting metal fill 334. Low-k dielectric is used [0037]-[0038]. Cu is used as the metal fill, a Cu seed is used and planarization by CMP is used [0042].

Burke lacks anticipation only in not explicitly teaching that the BARC layer 320 is a hard mask layer (HM1) (so that the bi-layered hard mask layer is made of HM1 and HM2); the BARC is formed with photoresist; the substrate is semiconductor single crystal silicon or an IC module; the hard mask layers are formed of SiN and SiC; the thicknesses of layers, the etching formula, repeating the steps to form multiple layers of interconnect, cu seed layer in the trench and via openings, forming excess copper metal over the copper seed layer and then planarizing the excess copper, and, MOSFET CMOS memory and logic devices.

7. Weidman teaches, in figures 1A-1H, and corresponding text, in a similar structure, a substrate 2 including insulating layer 6 with embedded conductor 4, IMD 16, bi-layered hard masks 20 and 22 (formed of SiC and/or SiN; [0009]) and an overlying BARC 24. The bi-layered hard mask and IMD layers are patterned and etched to form open via and trench openings (figs. 1E-1H) for subsequent conducting metal fill. The second hard mask is formed over the first hard mask in order to protect it [0030]-[0033].

Wang teaches, also in a similar structure, explicitly, that the BARC is a type of photoresist that does not have photosensitivity ([0025] – [0028]). The BARC is treated as a type of photoresist and even is removed with the overlying photoresist because of its resist/polymer material.

It would have been obvious to one of ordinary skill in the art to have used the bi-layered hardmask layer under and in addition to the BARC layer, in the method of Burke, as taught in the method of Weidman, with the motivation that the bi-layered hard mask provides a protective top layer over the bottom hard mask layer during subsequent etching and processing steps.

It would have been obvious to one of ordinary skill in the art to have had the substrate be formed of semiconductor single crystal silicon or an IC module, in the method of Burke, with the motivation that these materials are conventional substrate materials suitable to support the dielectric inlaid metal layer.

It would have been obvious to one of ordinary skill in the art to have had formed the BARC layer of photoresist and to have filled the via openings with photoresist, in the method of Burke, with the motivation that treated or specific types of photoresist are conventionally used as BARC layers and photoresist has also been commonly used to fill a via to facilitate patterning of an opening, especially of the damascene type in an insulating stack. The use of photoresist as a BARC film and to fill the via would make the process more efficient in that less materials would have to be used. Additionally, it would have been obvious to one of ordinary skill in the art to have formed the BARC of resist and to have filled the via openings with resist, in the method of Burke, with the motivation that Wang teaches that BARC is a type of photoresist which has been

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treated to not have the photosensitivity and, Wang even refers to the overlying photoresist as a second photoresist.

It would have been obvious to one of ordinary skill in the art to have had the claimed ranges of thicknesses of layers, and the claimed materials of the hard mask stack, the etching formula, to have repeated the steps to form multiple layers of interconnect and, to have had MOSFET CMOS memory and logic devices, in the method of Burke, with the motivation that Weidman teaches that the materials for hard masks may be combined differently according to the materials, and with the motivation that these parameters are within the scope of conventional processing parameters and well known to those of ordinary skill in the art, as is the inclusion of MOSFET CMOS memory and logic devices in the substrate beneath the interconnect is conventional as well and obvious to one of ordinary skill in the art. Also, see Wang for typical/conventional thicknesses of layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley  
Primary Patent Examiner  
TC 2800, Art Unit 2812

LAG  
July 22, 2006